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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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F. Chau & Associates, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,063	NAM ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-16,22 and 23* is/are rejected.

7)☒ Claim(s) *5-8 and 17-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 9, 11, 15, 16 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation, at lines 4-6 of claim 4 and at lines 26-27 of claim 15, "an arrangement of the plurality of first SACs forms a plurality of first rows having a plurality of second rows disposed in an alternating arrangement there between" is unclear to the Examiner. Further explanation in light of figure is requested.

The limitations, at lines 10-12 of claim 4 and at lines 7-8 of claim 15, "that is positioned along a same one of the plurality of columns as the one of the plurality of the second SACs" is unclear to the Examiner. Does it mean – contact plug 165 is positioned at the same column that of the second SACs 155b --? (refers to Fig. 11B)

The limitations, at lines 13-17 of claim 4 and at lines 12-15 of claim 15, " each of the plurality of bit lines respectively formed along one of the plurality of second rows and extending in a direction of the major axis, the plurality of second rows corresponding to areas having an absence of contact between any of the plurality of active regions and the top surface of any of the plurality of contact plugs" is unclear to the Examiner. Further explanation in light of figure is requested. Does it refer to Figs. 10 and 12B,wherein bit lines 180 are formed at rows where the active regions 115 are absent ?

The limitations, at lines 15-16 of claim 9, " at the same one of the plurality of columns as the one of the plurality of the second SACs" are unclear to the Examiner. Does it mean -- at the same columns as that of the second SACs 155b --, as illustrated in Fig.10?

The limitation, at lines 11-13 of claim 11, " forming photoresist patterns in a line shape at each of a plurality of rows where an absence exists of any formation of the plurality of active regions on the first interlayer insulating layer" is confusing. Does it mean -- forming photoresist patterns in a line shape on the first interlayer insulating layer at each of a plurality of rows where the plurality of active regions are absent --?

The limitations, at lines 19-26 of claim 16, "to respectively expose there through the sidewalls and the predetermined portion of the top surface of one of the plurality of second SACs, and the portion of the top surface of the isolation layer that is positioned at the same one of the plurality of columns as the one of the plurality of second SACs and at one of the plurality of second rows that precedes or follows one of the plurality of first rows within which lies the one of the plurality of second SACs", is narrative form and very confusing to the Examiner. Changing into "positive reciting" form (e.g. exposing the source/drain regions or positioning the A at the B region) is required.

The limitations, at lines 14-17 of claim 23, "positioned at either a first opposing side or a second opposing side of the isolation layer, the first opposing side and the second opposing side of the isolation layer being adjacent to at least one of the first side or the second side of at least one of the plurality of the gates" are unclear to the Examiner. A detailed explanation with the assistance of figure(s) is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 3, 10-13, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. (US 6,352,896).

In re claims 1 and 10, Liu et al., in Figs. 2A, 4I and related text, teach the claimed semiconductor device, comprising:

- a semiconductor substrate 200 (Fig. 4I);
- an isolation layer 202 formed on the semiconductor substrate 200 for defining a plurality of active regions 204 (Fig.2A and 4I), each of the plurality of active regions 204 having a major axis (X axis) and a minor axis (Y axis);
- a plurality of gates 206/210 and 208/210 formed to cross the plurality of active regions 204 (Fig.4I) and extend in a direction of the minor axis of each of the plurality of active regions 204, each of the plurality of gates 206/210 and 208/210 having a first side (left side) and a second side (right side) that are opposing and that run along the direction of the minor axis;
- a plurality of first and second source/drain regions (not shown but stated in col. 3, lines 49-51) formed in the plurality of active regions 204 at either of the first side or

the second side of each of the plurality of gates 206/210 and 208/210, each of the plurality of first and second source/drain regions having a top surface; and

- a plurality of first self-aligned contact pads (SACs) 222a and a plurality of second SACs 222b formed to contact the top surface of each of the plurality of first and second source/drain regions, respectively, wherein each of the plurality of first SACS 222a and each of the plurality of second SACs 222b are a same size (Fig. 4I).

In re claim 2, Liu et al also teach that the plurality of gates 206/210 and 208/210 are formed such that each two of the plurality of gates 206/210 crosses one of the plurality of active regions 204 (Fig.2A).

In re claim 3, Liu et al. also teach that the isolation layer 202 has a top surface, and said semiconductor device further comprises a plurality of third SACs 222b formed to contact areas of the top surface of the isolation layer 202 that are disposed between adjacent first SACs 222a in a direction of the major axis of each of the plurality of active regions 204 (Fig.4I).

In re claim 11, Liu et al. also teach the claimed method for manufacturing a semiconductor device (Figs. 2A-2C, 4A-4I and related text), comprising the steps of:

- forming an isolation layer 202 on a semiconductor substrate 200, the isolation layer 202 for defining a plurality of active regions 204, each of the plurality of active regions 204 having a major axis (X axis) and a minor axis (Y axis);
- forming a plurality of gates 206/210 and 208/210 on areas of the semiconductor substrate 200 on which the isolation layer 202 is formed, the plurality of gates 206/210 and 208/210 formed to cross the plurality of active regions 204 (Fig.2A) and extend in a direction of the minor axis (Y axis) of each of the plurality of active

regions 204, each of the plurality of gates 206/210 and 208/210 having a top surface and having a first side and a second side that are opposing and that that run along the direction of the minor axis;

- forming a plurality of first and second drain/source regions) (not shown) in the plurality active regions 204 at either of the first side or the second side of each of the plurality of gates 206/210 (col. 3,lines 49-51), each of the plurality of first and second source/drain regions having a top surface;
- forming a first interlayer insulating layer 216 on regions of the semiconductor substrate 200 on which the plurality of first and second source/drain regions are formed, the first interlayer insulating layer 216 formed to completely fill spaces among the plurality of gates 206/210 and 208/210 and to have a planarized top surface(Fig.4B);
- forming photoresist patterns 218 in a line shape at each of a plurality of rows where an absence exists of any formation of the plurality of active regions 204 on the first interlayer insulating layer 216 (Fig. 2C);
- etching the first interlayer insulating layer 216 using the photoresist patterns 218 as etching masks to form a plurality of contact holes 220a through which the top surface of each of the plurality of first and second source/drain regions are respectively exposed (Fig.3C);
- removing the photoresist patterns 218 (Fig.3D); and
- forming a plurality of first self-aligned contact pads (SACs) 222a and a plurality of second SACs 222b to respectively contact the top surface of each of the plurality of

first and second source/drain regions and to be level with the top surface of each of the plurality of gates 206/210 and 208/210, by filling the plurality of contact holes with a conductive material (Fig.4D).

In re claim 12, Liu et al. also teach that the plurality of gates 206/210 and 208/210 are formed such that each two of the plurality of gates 206/210 crosses one of the plurality of active regions 204 (Fig. 2A).

In re claim 13, Liu et al. also teach said step of forming the plurality of gates 206/210 and 208/210 comprises the steps of:

- sequentially forming a gate insulating layer (i.e. gate oxide, col.3, lines 34-36), a gate electrode 206 and 208, and a capping layer 210 on the areas of the semiconductor substrate 200 on which the isolation layer 202 is formed (Fig.4I);
- patterning the gate insulating layer, the gate electrode 206 and 208, and the capping layer 210 to form a patterned gate insulating layer, a patterned gate electrode, and a patterned capping layer; and
- forming gate spacers 212 to surround sidewalls of the patterned gate insulating layer, the patterned gate electrode, and the patterned capping layer, wherein the capping layer 210 and the gate spacers 212 are formed of an insulating material (silicon nitride) having a different etching selectivity from that of the first interlayer insulating layer (i.e. oxide) (col.4, lines 11-15).

In re claims 22 and 23, Liu et al. also teach that each of the photoresist patterns 218 are formed to include a protrusion as shown in Fig. 2C covering the first interlayer insulating layer 216 (Fig.4C), which is at the top surface of the isolation layer 202 positioned each of a plurality

of rows whereat the plurality of active regions 204 are formed (Figs. 2C and 4C); and the protrusion is formed to extend over any of the plurality of gates 206/210 and 208/210 that positioned at either a first opposing side or a second opposing side of the isolation layer 202, the first opposing side and the second opposing side of the isolation layer 202 being adjacent to at least one of the first side or the second side of at least one of the plurality of the gates 206/210 and 208/210.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US '896) in view of Hurley (US 2003/0013253).

Liu et al. teach the claimed limitations, as stated above, with the exception of forming a material layer that partially fills the spaces among the plurality of gates, subsequent to said step of forming the plurality of first and second source/drain regions, wherein the material layer is formed of an insulating layer having a different etching selectivity from that of the first interlayer insulating layer and is etched along with the first interlayer insulating layer.

Hurley in an analogous art teach forming a material layer 81 that partially fills the spaces among the plurality of gates 22/33/34/35/36 (Fig.8), subsequent to said step of forming the plurality of first and second source/drain regions 41 and 51, wherein the material layer 81 is formed of an insulating layer (i.e. titanium nitride barrier) having a different etching selectivity

from that of the first interlayer insulating layer 64 (BPSG) and is etched along with the first interlayer insulating layer 64 (Figs. 7-8).

Therefore, one of the ordinary skilled in the art, at the time the invention was made, would have been motivated to forming a material layer partially filling the spaces among the gate as taught by Hurley in the method Liu et al. since by doing so it would prevent the gates from over-etching.

Allowable Subject Matter

7. Claims 4, 9, 15 and 16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 5-8 and 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Liu et al. neither teach nor suggest forming a plurality of contact plugs through the first and the second interlayer insulating layers to respectively *contact the sidewalls and a predetermined portion of the top surface of each of the plurality of second SACs*; and forming a plurality of bit lines, each of the plurality of bit lines respectively formed along one of the plurality of second rows and extending in a direction of the major axis of each of the plurality of active regions, *the plurality of second rows corresponding to areas having an absence of contact between any of the plurality of active regions and a top surface of any of the plurality of contact plugs.*

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al. to US 6,479,355 (Figs.2A-2C and 3A) teach the common subject matters as recited in claims 1-3 and 10.

Ahn et al. to US 2001/0054719 Lee to US 2002/0070398 and Kamiya et al. to US 6,080,624 teach the common subject matters.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

May 29, 2003